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UTILIZING A BRIDGELESS BUCK BOOST CONVERTER FOR AN ADJUSTABLE SPEED POWER FACTOR CORRECTED (PFC) FED BLDC MOTOR DRIVE

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ABSTRACT- BLDC motors are used in a variety of industrial applications. These BLDC motor drivers are powered by various converter topologies. The topology of a bridgeless buck-boost converter with power factor correction (PFC) is proposed in this study for feeding a low-power brushless direct current (BLDC) motor drive. A bridgeless buck-boost converter that eliminates the requirement for a diode bridge rectifier and the accompanying conduction losses. Filters are frequently used with these converters to reduce harmonic distortion and improve power quality. Finally, the proposed drive's performance is simulated in the Matlab/Simulink environment, improving power quality at the ac mains.

Keywords: Power factor correction, BLDC motor, Bridgeless buck-boost converter, Total harmonic distortion

1. INTRODUCTION

Over the past decade, BLDC motors have been more popular due to their efficiency, power density, small size, ruggedness, low maintenance, and EMI avoidance [1-3]. Three-phase synchronous BLDC motors have DC speed and torque [1-3]. Stator has three-phase windings and rotor has fixed magnets. VSIs switch them on and off. It uses Hall Effect position sensors to measure rotor position for electrical commutation instead of brushes and a commutator assembly. This prevents sparking, brush wear, EMI, and noise interference in BLDC motors.

IEC 61000-3-2 requires improved power quality (PQ) for Class-A usage. This standard requires high power factor (PF) and low total harmonic distortion (THD) for ac mains current. Thus, power factor drops to 0.72 and AC mains source current has high total harmonic distortion. Better power quality converters (IPQC) improve AC mains power quality and reduce EMI. Many PFC converter topologies for BLDC motor drives have been described. Traditional BLDC motor drives with a front-end diode bridge rectifier (DBR) and a high-value DC link capacitor pull a lot of distorted current. Gopalarathnam et al. developed a SEPIC (Single Ended Primary Inductance Converter) to power BLDC motor drives using this principle. Its bifilar winding, PWM-based VSI control, and switching losses are excessive.Singh et al. propose a variable DC link voltage BLDC motor drive using a PFC Cuk converter. A Cuk converter that works in CCM requires three sensors, but it can handle more power and is better. Gopalarathnam et al. proposed a SEPIC (Single Ended Primary Inductance Converter) to power a BLDC motor. Its bifilar winding, PWM-based VSI control, and switching losses are excessive. Over the past decade, bridgeless converters have become more popular due to their efficiency. These designs reduce conduction losses by eliminating the front end DBR.

Power quality and total harmonic distortion are usually improved by these converters' filters. The appropriate mode of operation for PFC converters affects part pricing and compatibility. Converters can operate in CCM and DCM. DCM is mostly used in low-power situations. That's because CCM requires two sensors to monitor capacitor voltage and inductor current. DCM uses one monitor to measure DC link voltage. DC link voltage control isn't suitable for high-power applications since it stresses switches.

A BLDC motor-feeding buck–boost converter is suggested. It controls speed with PWM-VSI and a set dc link voltage, although switching losses are high. A buck–boost converter system is ideal for controlling a wide range of DC link voltage.Recommended converter reduces conduction losses.

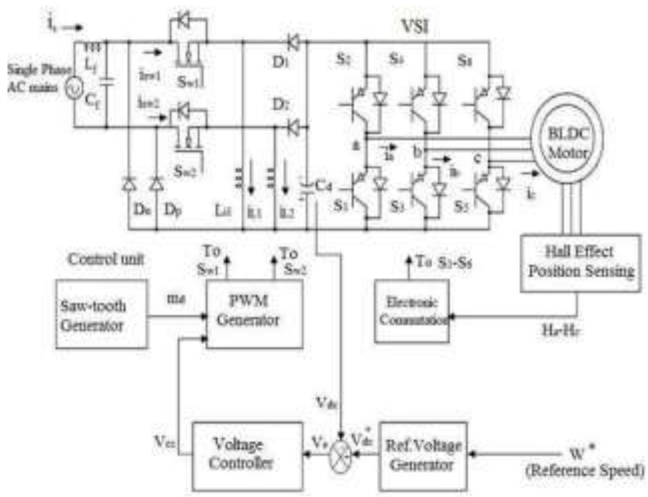

Fig. 1 BLDC motor transmission with PFC Buck-Boost converter.

2. PROPOSED BRIDGELESS BUCK-BOOSTCONVERTER FEEDING BLDC MOTOR DRIVE

The recommended converter uses "discrete inductor current." to reduce switching stress. Power quality is improved with a L filter at the input. One buck boost converter works during the positive half cycle and the other during the negative half cycle. The DC link capacitor always gives the drive three states per half cycle. Motor drives get alternating stator current from voltage source inverters. Electronic commutation manages inverter switches to adjust BLDC drive speeds. Converter filter voltage return control fixes power factor and voltage.

Every half-turn, the circuit functions three ways. Lf and Cf represent the input stage's filter inductance and capacitance. SW1 and Sw2 are switches, L1 and L2 are inductors, while D1 and D2 are diodes in the dual buck boost converter. The circuit also includes the BLDC motor drive with Hall Effect position (Ha-Hc) sensors and inverter switches S1–S6.

3. OPERATION OF BL BUCK BOOST CONVERTER

This converter handles positive and negative source voltage half cycles. Dual-buck boost converter. It runs in three states for each half cycle below.

Operation during the positive half cycle

This positive half-cycle activates the switch Sw1, inductor L1, and diodes Dp and D1. This transfers input energy to load.

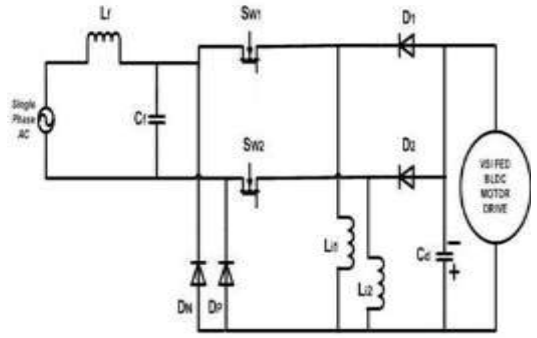

Fig. 2 We recommend this converter.

Mode1: Open switch Sw1 charges the inductor and increases iL1 current. Another circuit component is the diode Dp. The capacitor's energy will power the motor.

Mode2: The switch Sw1 is switched off, the inductor's current iL1 is dropped, and the saved energy is delivered to the DC link capacitor.

Mode 3: The switch and diode did not conduct electricity during this period. The inductor enters the interrupted phase when its current drops to zero. DC connection capacitor Cd sends stored energy to the load. After flipping, Switch Sw1 opens and closes again. This improves AC mains power.

Operation during the negative half cycle.

During this half cycle, diodes Dn and D2 and the switch Sw 2 transfer energy from input to load.

Mode 1: Open switch Sw2 charges the inductor and increases iL2 current. The diode Dn completes the circuit. The capacitor's energy will power the motor.

Mode 2: The switch Sw2 is switched off, the inductor's current iL2 is dropped, and the saved energy is delivered to the DC link capacitor.

Mode 3: The switch and diode did not conduct electricity during this period. The inductor enters the DCM when its current stops. The DC link capacitor Cd will feed the load its conserved energy. Switch Sw2 conducts after swapping.

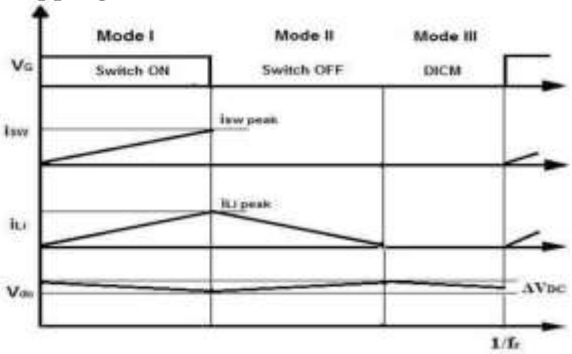

Fig. 5 Waveform showing half-cycle operation mode

4. CONTROL OF POWER FACTOR CORRECTED BRIDGELESS BUCK BOOST CONVERTER

Control of PFC Converter

DICM-mode converters are controlled by voltage followers. PWM signals for switches Sw1 and Sw2 are made by comparing the DC link voltage with a reference signal. Baseline signal is made to

$$V_{dc}^{*} = k_v w^{*}$$

Kv represents the motor's constant voltage, while w* represents its normal speed. Comparing this DC link voltage to the usual DC link voltage generates a problem signal.

$$V_e = V_{dc}^{*} - V_{dc}$$

The PI processor generates the control output voltage from the error signal. This output control voltage is compared to a high-frequency sawtooth wave to generate PWM pulses.

If Vs> 0,

If md<Vcc , then Sw1 ON If md≥Vcc then Sw1 OFF

If Vs< 0,

If md<Vcc , then Sw2 ON If md ≥ Vcc , then Sw2 OFF

Sw1 and Sw2 are the switching signals.

Electronic Commutation

For electronic commutation, the VSI switches must be adjusted to draw a balanced current from the DC link capacitor for 1200 and put it down evenly at each phase. To locate the rotor, use a Hall effect position monitor. Based on this, a decoder provides gating signals to the inverter switches and turns on the right switches from the upper and lower limbs to conclude current flow and turn on the stator windings. The table shows the VSI switching procedure and Hall Effect position sensor condition.

Different frequencies are detected by sound sensors. Decoding their active state modifications allows the following switching series. The upper limb switches are connected to the higher voltage side, hence a bootstrap-oriented gate control is needed.

Table 1 Electrical commutation state changes based on hall sensor output signals

Hall Signals			Switching Sequence					
Ha	Hb	Hc	S1	S2	S3	S4	S5	S6
0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	0	0	1	1	0
1	0	1	1	0	0	1	0	0
1	1	0	0	1	0	0	1	0
1	1	1	0	0	0	0	0	0

5.SIMULATION RESULTS

MATLAB/Simulink's Sim-Power-System toolbox models the planned BLDC motor drive's performance. We evaluate the suggested drive's performance based on the BLDC motor, BL buck boost converter, and AC mains power quality. Speed, electromagnetic torque, and stator current affect BLDC motor performance. Supply voltage, current, DC link voltage, inductor currents, switch voltages, and switch currents are examined to ensure the PFC BL buck boost converter functions properly. PF (Power Factor) and THD (Total Harmonic Distortion) of the source current are also used to assess AC mains power quality. Results of the experiment are below.

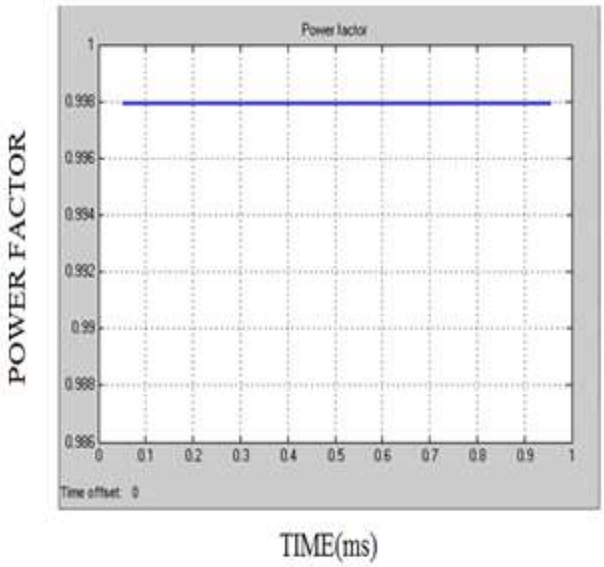

Fig. 7 Power factor follows power quality.

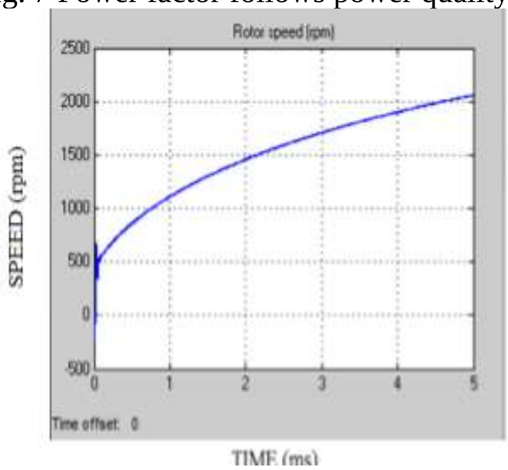

Fig. 8 Rotor speed performance

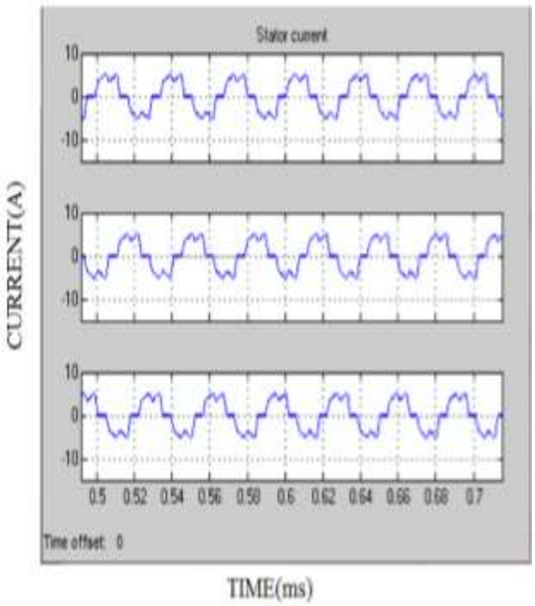

Fig. 9 Three phase BLDC Stator current

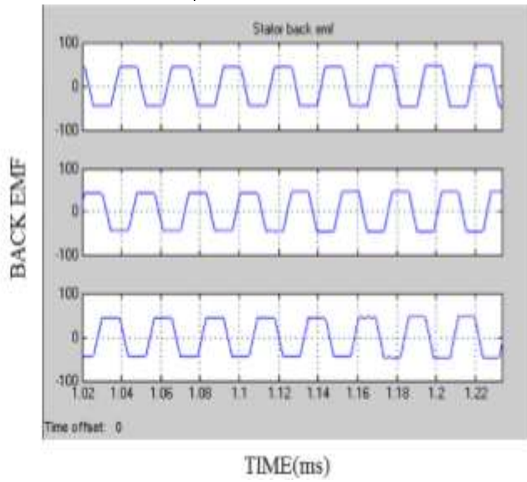

Fig. 10 Backward three-phase BLDC Stator electrical force

6.COMPARATIVE ANALYSIS OF PROPOSED AND EXISTING SYSTEM

The proposed mechanism functioned well enough to be valid.

Table 2 Current System Performance and Speed with PFC (CUK converter fed BLDC drive)

Vdc	40	60	80	100	120	140
Speed	380	580	790	990	1210	1410
Power Factor	0.998	0.998	0.998	0.998	0.998	0.998

Table 3 PFC and speed of the recommended system (a BLDC drive supplied by a BL Buck-BOOST converter)

Vdc	40	60	80	100	120	140
Speed	380	580	790	990	1210	1410
Power factor	0.99	0.99	0.99	0.99	0.99	0.99

7.CONCLUSION

This study simulates a low-power bridgeless buck-boost converter feeding a BLDC motor drive. The converter may improve AC mains power. This arrangement can boost power factor to 0.99. alter the DC bus voltage to alter BLDC motor speed. Electronic commutation reduces inverter switching strain. Power variations in the DC link can control speed. Future isolation networks could block electric power from flowing without permission, and dynamic load change monitors could detect rapid load changes.

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